What is claimed is:

1. A method of forming a FinFET, comprising the steps of:
forming a set of at least one semiconducting fin on a substrate;
forming a gate insulator on said set of fins;
depositing a layer of gate material over said set of fins;
forming a hardmask on said gate material extending perpendicular to said set of fins and having a hardmask thickness;
etching said gate material outside said hardmask down to said substrate, thereby forming a gate intersecting said set of fins and defining a body region in said fins below said gate;
depositing a conformal layer of insulator enclosing said gate;
performing an anisotropic etch of said conformal layer, thereby exposing said set of fins while said gate remains covered by said conformal layer of insulator; and
forming source and drain regions in said fins, separated from said gate by said conformal layer of insulator.

2. A method according to claim 1, further comprising the steps of:
depositing a source/drain material over a set of at least two fins after said anisotropic etch of said conformal layer, thereby making contact with sides of said at least two fins and forming a FinFET having at least two fins.

3. A method according to claim 2, further comprising a step of:
recessing said source/drain material to substantially the height of said set of fins; and

forming source/drain contacts on a top surface of said source/drain material.

4. A method according to claim 2, in which said fins and said gate are formed from silicon and further comprising the steps of:
exposing silicon in said fins and in an upper portion of said gate; and
performing a silicidation step of said exposed silicon.

5. A method according to claim 2, further comprising the steps of:
depositing a blocking material over a set of FinFET locations and opening an aperture over a subset of locations for a first polarity of FinFETs;
depositing a second conformal insulating layer over gates in said locations for a first polarity of FinFETs, said second layer having a separation thickness combined with said first layer such that dopant material in sources and drains of said first polarity of FinFETs are separated from said gates.

6. A method according to claim 2, in which:
said hardmask thickness is such that a remaining layer of said hardmask remains above said gate after said anisotropic etch when said fins are exposed by removing said conformal layer of insulator down to said substrate.

7. A method according to claim 1, in which said fins and said gate are formed from silicon and further comprising the steps of:
exposing silicon in said fins and in an upper portion of said gate; and
performing a silicidation step of said exposed silicon.

8. A method according to claim 1, further comprising the steps of:
depositing a blocking material over FinFET locations and opening an aperture over locations for a first polarity of FinFETs;
depositing a second conformal insulating layer over gates in said locations for a first polarity of FinFETs, said second layer having a separation thickness combined with said first layer such that dopant material in sources and drains of said first polarity of FinFETs are separated from said gates.

9. A method according to claim 8, further comprising the steps of:
depositing a source/drain material over a set of at least two fins after said anisotropic etch of said conformal layer, thereby making contact with sides of said at least two fins and forming a FinFET having at least two fins.

10. A method according to claim 9, in which;
said hardmask thickness is such that a remaining layer of said hardmask remains above said gate after said anisotropic etch when said fins are exposed by removing said conformal insulating layer down to said substrate.

11. A method according to claim 9, in which said fins, said S/D material and said gate are formed from silicon and further comprising the steps of:
exposing silicon in said fins and S/D material and in an upper portion of said gate; and
performing a silicidation step of said exposed silicon.

12. A method according to claim 11, further comprising a step of:

after said step of silicidation, removing said conformal layer over said gate, thereby forming an aperture between said gate and said S/D material having a vertical exposed silicon gate surface; and
performing a step of silicidation on said exposed gate surface.

13. A method according to claim 1, in which;
said hardmask thickness is such that a remaining layer of said hardmask remains above said gate after said anisotropic etch when said fins are exposed by removing said conformal insulating layer down to said substrate.

14. A method according to claim 13, in which;
said hardmask thickness is such that a remaining layer of said hardmask remains above said gate after said anisotropic etch when said fins are exposed by removing said conformal insulating layer down to said substrate.

15. A method according to claim 13, in which said fins, said S/D material and said gate are formed from silicon and further comprising the steps of:
exposing silicon in said fins and S/D material and in an upper portion of said gate; and
performing a silicidation step of said exposed silicon.

16. A method according to claim 15, further comprising a step of:
after said step of silicidation, removing said conformal layer over said gate, thereby forming an aperture between said gate and said S/D material having

a vertical exposed silicon gate surface; and
performing a step of silicidation on said exposed gate surface.

17. A method according to claim 2, in which said fins, said S/D material and said gate are formed from silicon and further comprising the steps of:
exposing silicon in said fins and S/D material and in an upper portion of said gate; and
performing a silicidation step of said exposed silicon.

18. A method according to claim 17, further comprising a step of:
after said step of silicidation, removing said conformal layer over said gate, thereby forming an aperture between said gate and said S/D material having a vertical exposed silicon gate surface; and
performing a step of silicidation on said exposed gate surface.

19. An integrated circuit comprising at least one FinFET comprising:
a set of at least one semiconducting fin(s) on a substrate;
said set of fins having a gate insulator separating a body region thereof from a selfaligned gate formed by etching a layer of gate material disposed over said set of fins outside a hardmask down to said substrate, thereby forming a gate intersecting said set of fins and defining said body region in said fins below said gate;
a separation layer of insulator enclosing said gate and formed by an anisotropic etch of a conformal layer, that exposed said set of fins while said gate remained covered by said conformal layer of insulator; and
source and drain regions in said fins, selfaligned to said gate and separated

from said gate by said conformal layer of insulator.

20. An integrated circuit according to claim 19, in which said set of fins comprises at least two fins having a source portion and a drain portion, at least one of which source and drain portions are in electrical contact with a S/D material on vertical sides thereof.

21. An integrated circuit according to claim 20, in which said S/D material is recessed below a top of said gate and above a top of said fins.

22. An integrated circuit according to claim 21, in which said S/D material is silicon and a portion thereof is silicide.

23. An integrated circuit according to claim 19, in which a first subset of N-type FinFETs has a first thickness of said separation layer and a second subset of P-type FinFETs has a second thickness of separation layer, said second thickness being greater than said first thickness.